FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10153-5E

MEMORY

CMOS

256K × 16 BIT FAST PAGE MODE DYNAMIC RAM

MB81V4260S-60/-70

CMOS 262,144 × 16 Bit Fast Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB81V4260S is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 16-bit increments. The MB81V4260S features a “fast page” mode of operation whereby high-speed access of up to 512×16-bits of data can be selected in the same row. The MB81V4260S-60/-70 DRAMs are ideally suited for memory applications such as embedded control, buffer, portable computers, and video imaging equipment where very low power dissipation and high bandwidth are basic requirements of the design.

The MB81V4260S is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon process. This process, coupled with three-dimensional stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes.

■ PRODUCT LINE & FEATURES

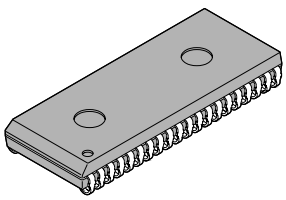
Parameter		MB81V4260S-60	MB81V4260S-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
$\overline{CAS}$ Access Time		20 ns max.	20 ns max.
Address Access Time		30 ns max.	35 ns max.
Random Cycle Time		110 ns max.	125 ns min.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Low Power Dissipation	Operating current	378 mW max.	335 mW max.
	Standby current	7.2 mW max. (LVTTL level),3.6 mW max. (CMOS level)	

- Low V_{CC} operating
- 262,144 words × 16 bit organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are LVTTL comaptible
- 512 refresh cycles every 8.2 ms
- 9 rows × 9 columns, refresh addressing scheme
- Self refresh function
- 1$\overline{WE}$ / 2$\overline{CAS}$
- Early Write or $\overline{OE}$ controlled Write capability
- $\overline{RAS}$ only $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

MB81V4260S-60/MB81V4260S-70

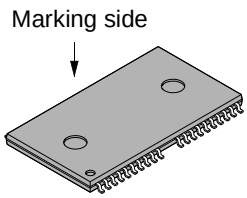
■ PACKAGE

Plastic SOJ Package

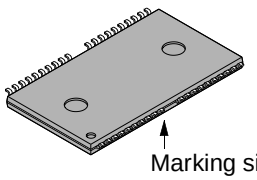


(LCC-40P-M01)

Plastic TSOP (II) Packages



(FPT-44P-M07)
(Normal Bend)



(FPT-44P-M08)
(Reverse Bend)

Package and Ordering Information

– 40-pin plastic (400 mil) SOJ, order as MB81V4260S-××PJ

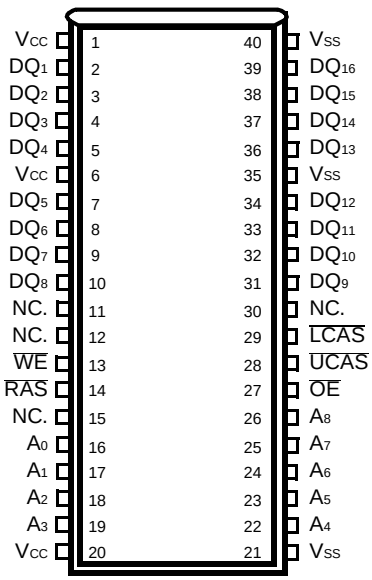
– 44-pin plastic (400 mil) TSOP-II with normal bend leads, order as MB81V4260S-××PFTN

– 44-pin plastic (400 mil) TSOP-II with reverse bend leads, order as MB81V4260S-××PFTR

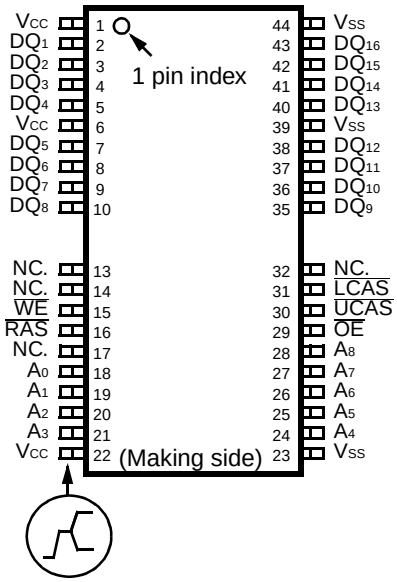
MB81V4260S-60/MB81V4260S-70

■ PIN ASSIGNMENTS AND DESCRIPTIONS

40-Pin SOJ:
(TOP VIEW)
<LCC-40P-M01>



44-Pin TSOP (II):
(TOP VIEW)
<Normal Bend : FPT-44P-M07>



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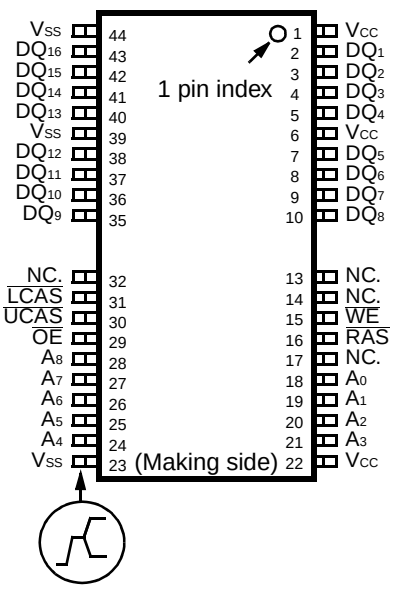
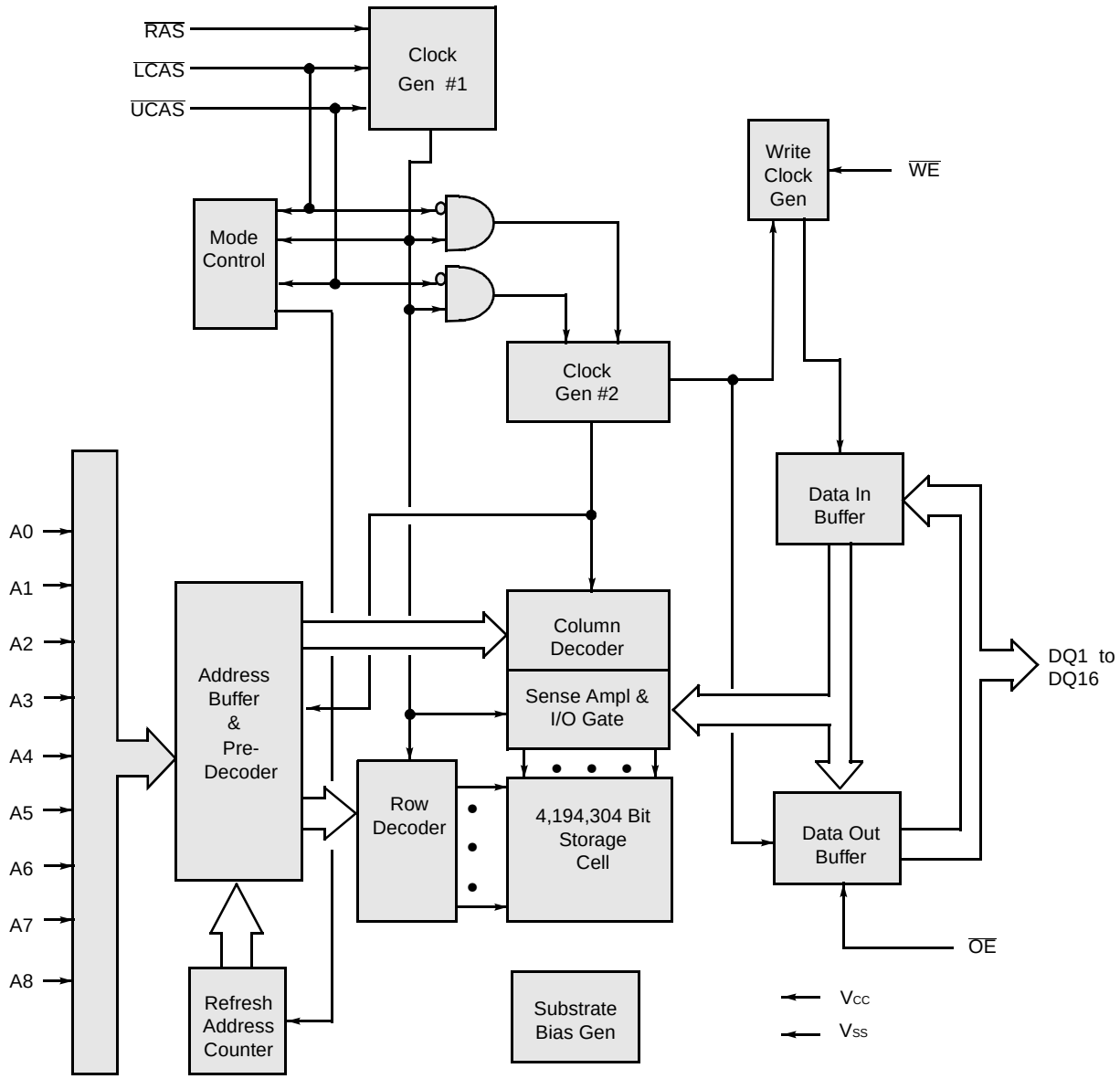


Designator	Function
A_0 to A_8	Address inputs. row : A_0 to A_8 column : A_0 to A_8 refresh : A_0 to A_8
$\overline{RAS}$	Row address strobe.
$\overline{LCAS}$	Lower column address strobe
$\overline{UCAS}$	Upper column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable.
DQ_1 to DQ_{16}	Data Input/ Output
V_{CC}	+3.3 volt power supply.
V_{SS}	Circuit ground.

MB81V4260S-60/MB81V4260S-70

■ BLOCK DIAGRAM

Fig. 1 – MB81V4260S DYNAMIC RAM - BLOCK DIAGRAM



■ FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address		Input/Output Data				Refresh	Note
								DQ_1 to DQ_8		DQ_9 to DQ_{16}			
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Row	Column	Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min.)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min.)
Read-Modify-Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	
$\overline{RAS}$-only Refresh Cycle	L	H	H	X	X	Valid	—	—	High-Z	—	High-Z	Yes	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	L	L	L	X	X	—	—	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min.)
Hidden Refresh Cycle	H→L	L H L	H L L	H	L	—	—	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept.

■ FUNCTIONAL OPERATION

ADDRESS INPUTS

Eighteen input bits are required to decode any sixteen of 4,194,304 cell addresses in the memory matrix. Since only nine address bits are available, the column and row inputs are separately strobed by $\overline{LCAS}$ or $\overline{UCAS}$ and $\overline{RAS}$ as shown in Figure 5. First, nine row address bits are input on pins A_0-through-A_8 and latched with the row address strobe ($\overline{RAS}$) then, nine column address bits are input and latched with the column address strobe ($\overline{LCAS}$ or $\overline{UCAS}$). Both row and column addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$, respectively. The address latches are the flow-through type; thus, address information appearing after t_{RAH} (min.)+ t_T is automatically treated as the column address to start select operation of the column decode. Therefore, to have correct data within t_{RAC}, the column address should be input within t_{RAD}(max.). If $t_{RAD} > t_{RAD}$(max.), the access time is the later one of either t_{AA} or t_{CAS}.

WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data are ignored. When an early write cycle is executed, the output buffers stay in a high-impedance state during the cycle.

DATA INPUT

Input data are written into memory in either of three basic ways–the early write cycle, the $\overline{OE}$ (delayed) write cycle, and the read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{LCAS}$/$\overline{UCAS}$, whichever is later, serves as the input data-latch strobe. In the early write cycle, the input data of DQ_1-DQ_8 are strobed by $\overline{LCAS}$ and DQ_9-DQ_{16} are strobed by $\overline{UCAS}$ and the setup/hold times are referenced to each falling edge of $\overline{LCAS}$ and $\overline{UCAS}$ because $\overline{WE}$ goes Low before $\overline{LCAS}$/$\overline{UCAS}$. In the delayed write or read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{LCAS}$/$\overline{UCAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the falling edge of $\overline{WE}$. Since this device is an I/O common type, when the delayed write or read-modified-write is executed, I/O data have to be controlled by $\overline{OE}$.

DATA OUTPUT

The three-state buffers are LVTTL compatible with a fanout of one TTL load. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t_{RAC} : from the falling edge of $\overline{RAS}$ when t_{RCD} (max.) is satisfied.
- t_{CAC} : from the falling edge of $\overline{LCAS}$ (for DQ_1-DQ_8) $\overline{UCAS}$ (for DQ_9-DQ_{16}) when t_{RCD} is greater than t_{RCD} (max.).
- t_{AA} : from column address input when t_{RAD} is greater than t_{RAD} (max.).
- t_{OEA} : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA}.

The data remains valid until either $\overline{LCAS}$/$\overline{UCAS}$ or $\overline{OE}$ returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 512×16-bits can be accessed. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or ready-modify-write cycles are permitted.

■ ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to V_{SS}	V_{IN}, V_{OUT}	–0.5 to +4.6	V
Voltage of V_{CC} supply relative to V_{SS}	V_{CC}	–0.5 to +4.6	V
Power Dissipation	P_D	1.0	W
Short Circuit Output Current	I_{OUT}	50	mA
Storage Temperature	T_{STG}	–55 to +125	°C
Temperature under Bias	T_{BIAS}	0 to +70	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp
Supply Voltage	*1	V_{CC}	3.0	3.3	3.6	V	0°C to +70°C
		V_{SS}	0	0	0		
Input High Voltage, all inputs	*1	V_{IH}	2.0	—	V_{CC}+0.3	V	
Input Low Voltage, all inputs(*)	*1	V_{IL}	–0.3	—	0.8	V	
Input Low Voltage, DQ(*)	*1	V_{ILD}	–0.3	—	0.8	V	

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance, A_0 to A_8	C_{IN1}	—	5	pF
Input Capacitance, $\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	C_{IN2}	—	7	pF
Input/Output Capacitance, DQ_1 to DQ_{16}	C_{DQ}	—	7	pF

MB81V4260S-60/MB81V4260S-70

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3

Parameter	Notes		Symbol	Conditions	Value		Unit
					Min.	Max.	
Output high voltage	*1		V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
Output low voltage	*1		V_{OL}	I_{OL} = +2.0 mA	—	0.4	
Input leakage current (any input)			$I_{I(L)}$	0 V ≤ V_{IN} ≤ 3.6 V; 3.0 V ≤ V_{CC} ≤ 3.6 V; V_{SS} = 0 V; All other pins not under test = 0 V	–10	10	µA
Output leakage current			$I_{DQ(L)}$	0 V ≤ V_{OUT} ≤ 3.6 V; Data out disabled	–10	10	
Operating current (Average power supply current)	*2	MB81V4260S-60	I_{CC1}	$\overline{RAS}$ & $\overline{LCAS}$, $\overline{UCAS}$ cycling; t_{RC} = min.	—	105	mA
		MB81V4260S-70				93	
Standby current (Power supply current)		LVTTL level	I_{CC2}	$\overline{RAS}$ = $\overline{LCAS}$, $\overline{UCAS}$ = V_{IH}	—	2.0	mA
		CMOS level		$\overline{RAS}$ = $\overline{LCAS}$, $\overline{UCAS}$ ≥ V_{CC} –0.2 V		1.0	
Refresh current #1 (Average power supply current)	*2	MB81V4260S-60	I_{CC3}	$\overline{LCAS}$, $\overline{UCAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min.	—	105	mA
		MB81V4260S-70				93	
Fast Page Mode current	*2	MB81V4260S-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{LCAS}$, $\overline{UCAS}$ cycling; t_{PC} = min.	—	105	mA
		MB81V4260S-70				93	
Refresh current #2 (Average power supply current)	*2	MB81V4260S-60	I_{CC5}	$\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min.	—	105	mA
		MB81V4260S-70				93	
Refresh current #3 (Average power supply current)	*2		I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = V_{IL} Self Refresh; t_{RASS} = min.	—	1000	µA

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		t_{RC}	110	—	125	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	150	—	170	—	ns
4	Access Time from $\overline{RAS}$	*6, 9	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	*7, 9	t_{CAC}	—	20	—	20	ns
6	Column Address Access Time	*8, 9	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	0	—	0	—	ns
8	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	*10	t_{OFF}	—	15	—	15	ns
10	Transition Time		t_T	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	45	—	ns
12	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
13	$\overline{RAS}$ Hold Time		t_{RSH}	20	—	20	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*11, 12	t_{RCD}	20	40	20	50	ns
16	$\overline{CAS}$ Pulse Width		t_{CAS}	20	10000	20	10000	ns
17	$\overline{CAS}$ Hold Time		t_{CSH}	60	—	70	—	ns
18	$\overline{CAS}$ Precharge Time (Normal)	*19	t_{CPN}	10	—	10	—	ns
19	Row Address Setup Time		t_{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
21	Column Address Setup Time		t_{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t_{CAH}	12	—	12	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	*13	t_{RAD}	15	30	15	35	ns
24	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
25	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	30	—	35	—	ns
26	Read Command Setup Time		t_{RCS}	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{RAS}$	*14	t_{RRH}	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{CAS}$	*14	t_{RCH}	0	—	0	—	ns
29	Write Command Setup Time	*15	t_{WCS}	0	—	0	—	ns
30	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
31	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
32	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	20	—	ns

(Continued)

MB81V4260S-60/MB81V4260S-70

(Continued)

No.	Parameter	Notes	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
				Min.	Max.	Min.	Max.	
33	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	15	—	18	—	ns
34	DIN Setup Time		t_{DS}	0	—	0	—	ns
35	DIN Hold Time		t_{DH}	10	—	10	—	ns
36	$\overline{RAS}$ to $\overline{WE}$ Delay Time		t_{RWD}	85	—	95	—	ns
37	$\overline{CAS}$ to $\overline{WE}$ Delay Time		t_{CWD}	40	—	40	—	ns
38	Column Address to $\overline{WE}$ Delay Time		t_{AWD}	55	—	60	—	ns
39	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh cycles)		t_{RPC}	10	—	10	—	ns
40	$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CSR}	0	—	0	—	ns
41	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh		t_{CHR}	10	—	10	—	ns
42	Access Time from $\overline{OE}$	*9	t_{OEA}	—	20	—	20	ns
43	Output Buffer Turn Off Delay from $\overline{OE}$	*10	t_{OEZ}	—	15	—	15	ns
44	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
45	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	*16	t_{OEH}	0	—	0	—	ns
46	$\overline{OE}$ to Data in Delay Time		t_{OED}	15	—	15	—	ns
47	DIN to $\overline{CAS}$ Delay Time	*17	t_{DZC}	0	—	0	—	ns
48	DIN to $\overline{OE}$ Delay Time	*17	t_{DZO}	0	—	0	—	ns
50	Column Address Hold Time from $\overline{RAS}$		t_{AR}	32	—	32	—	ns
51	Write Command Hold Time from $\overline{RAS}$		t_{WCR}	30	—	30	—	ns
52	DIN Hold Time Referenced to $\overline{RAS}$		t_{DHR}	30	—	30	—	ns
53	$\overline{CAS}$ to Data in Delay Time		t_{CDD}	15	—	15	—	ns
60	Fast Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	60	200000	70	200000	ns
61	Fast Page Mode Read/Write Cycle Time		t_{PC}	40	—	45	—	ns
62	Fast Page Mode Read-Modify-Write Cycle Time		t_{PRWC}	80	—	90	—	ns
63	Access Time from $\overline{CAS}$ Precharge	*9, 18	t_{CPA}	—	35	—	40	ns
64	Fast Page Mode $\overline{CAS}$ Pulse width		t_{CP}	10	—	10	—	ns
65	Fast Page Mode $\overline{RAS}$ Hold Time from CAS Precharge		t_{RHCP}	35	—	40	—	ns
66	Fast Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time		t_{CPWD}	55	—	60	—	ns

Notes: *1. Referenced to V_{SS}. To all V_{CC} (V_{SS}) pins, the same supply voltage should be applied.

*2. I_{CC} depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$= V_{IL} and $\overline{UCAS}$ = V_{IH}, $\overline{LCAS}$= V_{IH}, V_{IL} > –0.3V.
I_{CC1}, I_{CC3} and I_{CC5} are specified at one time of address change during $\overline{RAS}$= V_{IL} and $\overline{UCAS}$= V_{IH}, $\overline{LCAS}$= V_{IH}.
I_{CC4} is specified at one time of address change during one Page cycle.

*3. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

*4. AC characteristics assume t_T = 5 ns.

*5. Input voltage levels are 0V and 3.0V, and input reference levels are V_{IH}(min.) and V_{IL}(max.) for measuring timing of input signals. Also, the transition time (t_T) is measured between V_{IH}(min.) and V_{IL}(max.). The output reference levels are V_{OH} = 2.0 V and V_{OL} = 0.8 V.

*6. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.

*7. If $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*8. If $t_{RAD} \geq t_{RAD}$ (max.) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*9. Measured with a load equivalent to one TTL loads and 100 pF.

*10. t_{OFF} and t_{OEZ} is specified that output buffer change to high impedance state.

*11. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. t_{RCD} (min.) = t_{RAH} (min.) + 2t_T + t_{ASC} (min.).

*13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min.) the data output pin will remain High-Z state through entire cycle.

*16. Assumes that $t_{WCS} < t_{WCS}$ (min.).

*17. Either t_{DZC} or t_{DZO} must be satisfied.

*18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both $\overline{UCAS}$ and $\overline{LCAS}$ from “L” to “H”). Therefore, if t_{CP} is long, t_{CPA} is longer than t_{CPA} (max.).

*19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.

MB81V4260S-60/MB81V4260S-70

Fig. 2 – t_{RAC} vs. t_{RCD}

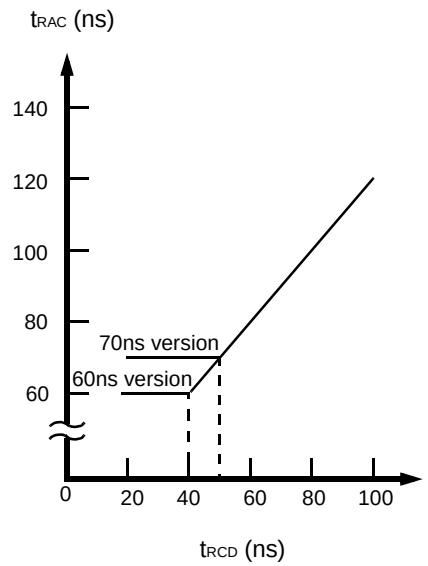


Fig. 3 – t_{RAC} vs. t_{RAD}

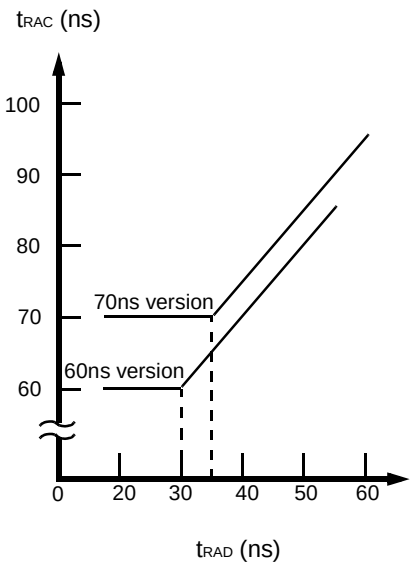
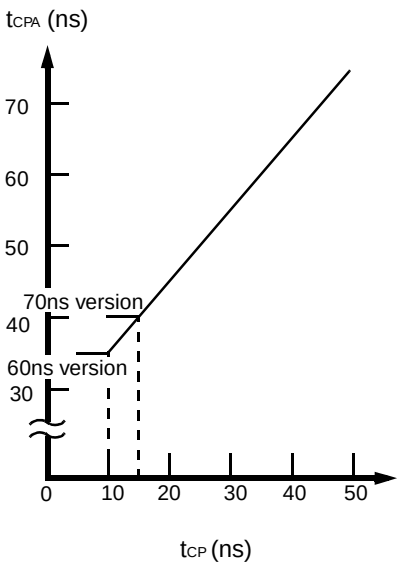
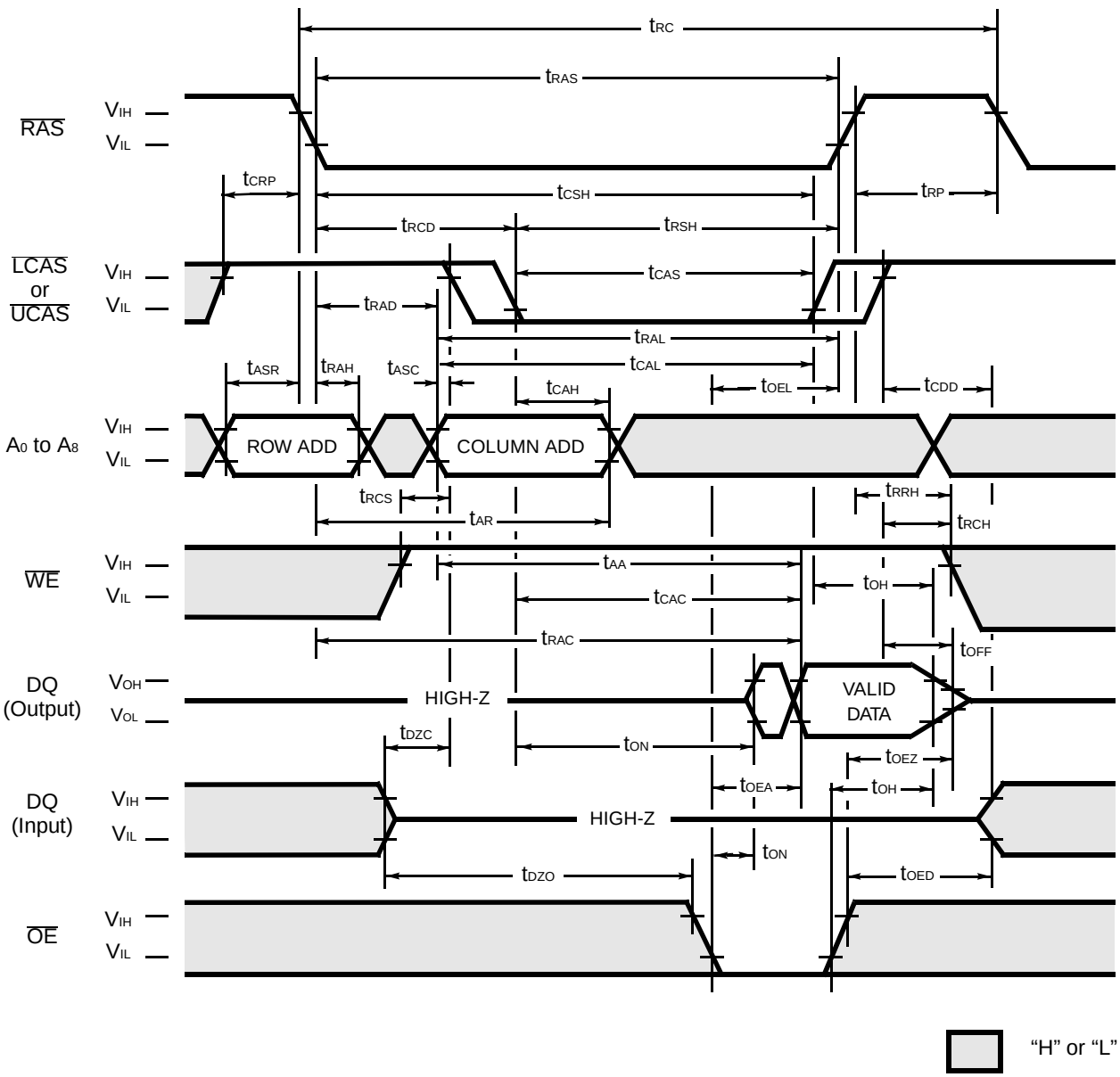


Fig. 4 – t_{CPA} vs. t_{CP}



X: "H" or "L"
*: It is impossible in Fast Page Mode.

Fig. 5 – READ CYCLE



DESCRIPTION

To implement a read operation, a valid address is latched in by the $\overline{RAS}$ and $\overline{LCAS}$ or $\overline{UCAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a low level, the output is valid once the memory access time has elapsed. $\overline{LCAS}$ controls the input/output data on DQ_1-DQ_8 pins, $\overline{UCAS}$ controls one on DQ_8-DQ_{16} pins. The access time is determined by $\overline{RAS}$(t_{RAC}), $\overline{LCAS}$/$\overline{UCAS}$ (t_{CAC}), $\overline{OE}$ (t_{OEA}) or column addresses (t_{AA}) under the following conditions:

If $t_{RCD} > t_{RCD}$ (max.), access time = t_{CAC}.

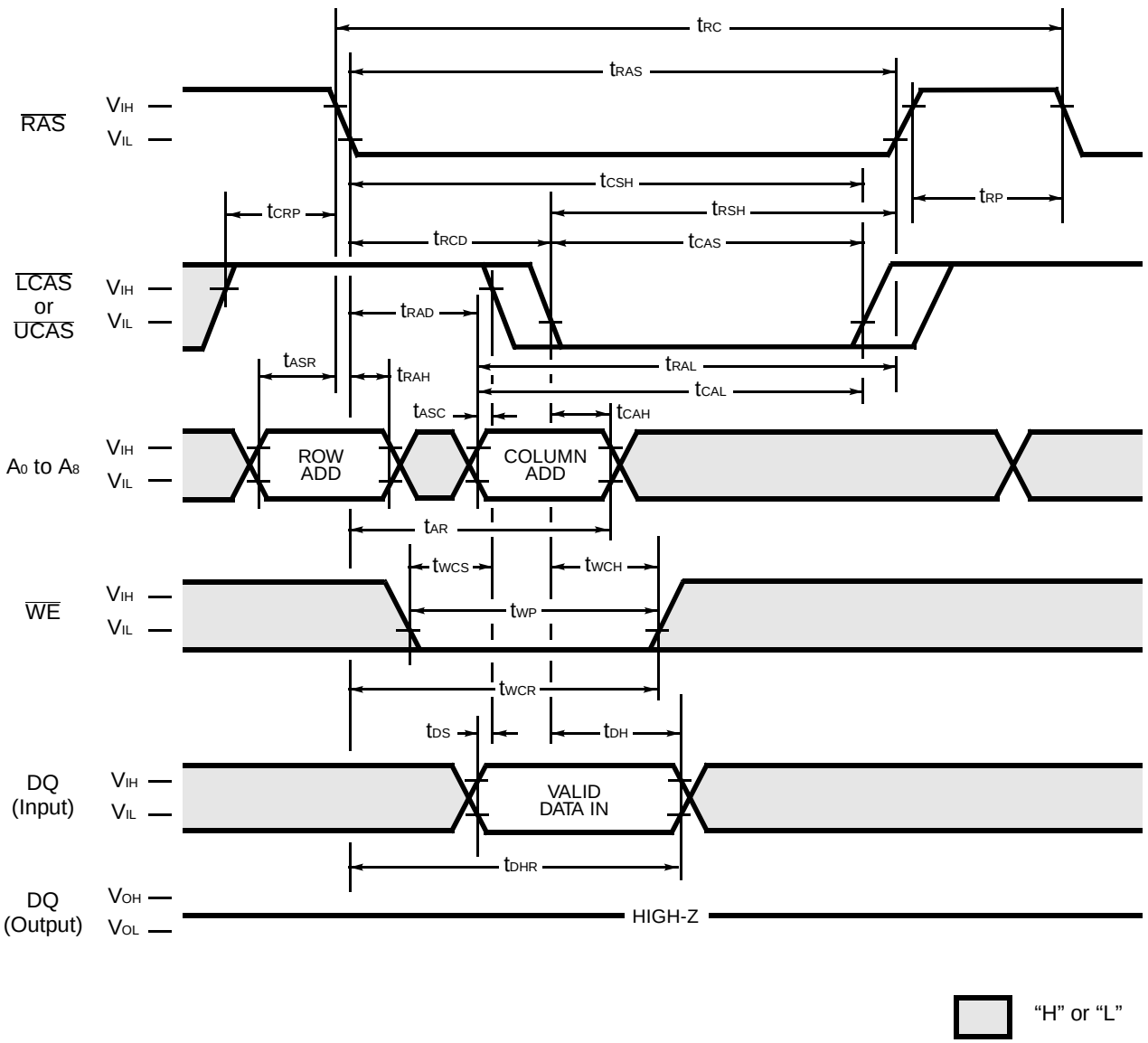
If $t_{RAD} > t_{RAD}$ (max.), access time = t_{AA}.

If $\overline{OE}$ is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (whichever occurs later), access time = t_{OEA}.

However, if either $\overline{LCAS}$/$\overline{UCAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after t_{OH} is satisfied.

MB81V4260S-60/MB81V4260S-70

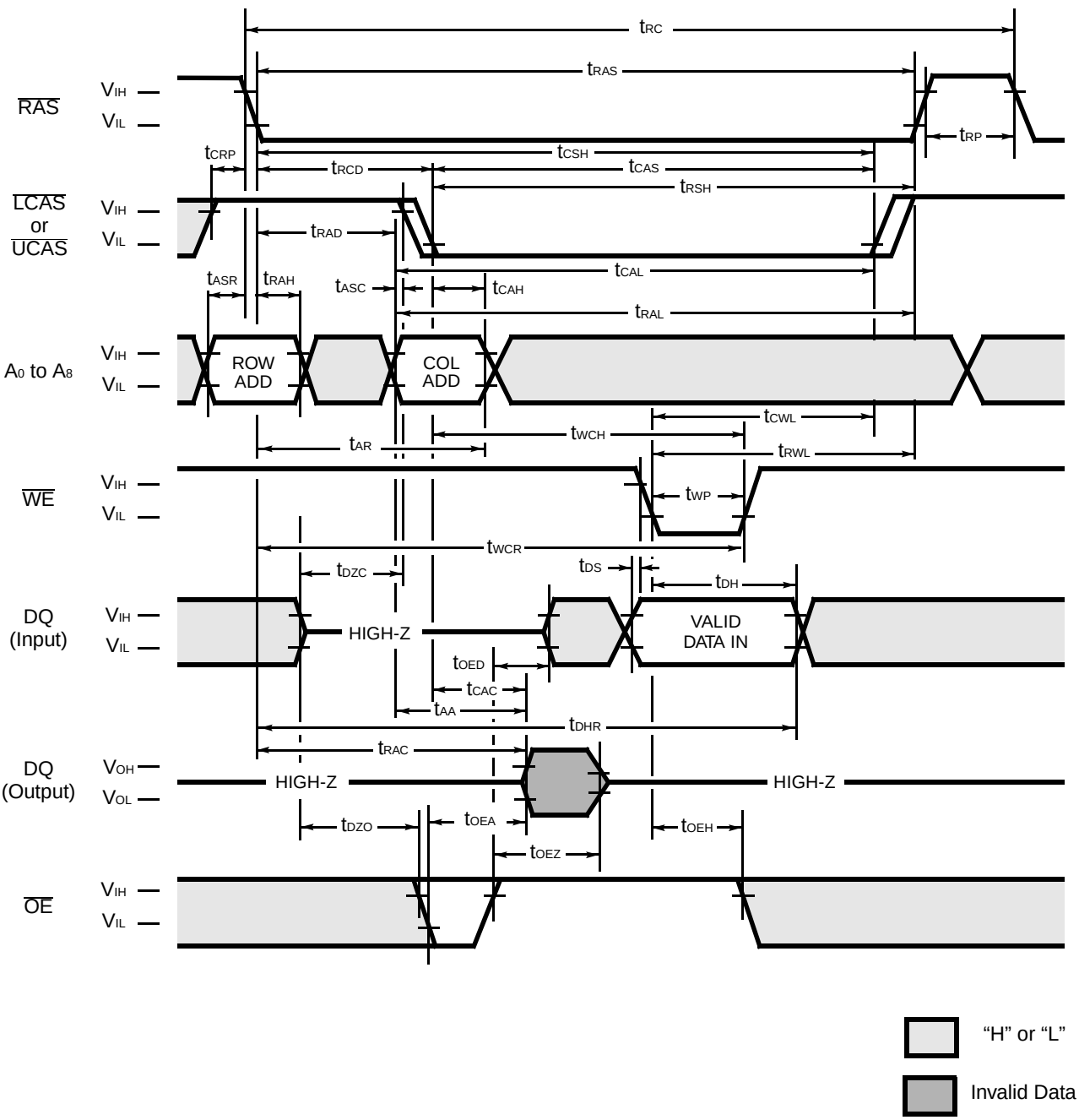
Fig. 6 – EARLY WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and $\overline{OE}$ is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, $\overline{OE}$ write (delayed write), or read-modify-write. During all write cycles, timing parameters t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} satisfied, data on the DQ pins are latched with the falling edge of $\overline{LCAS}$ or $\overline{UCAS}$ and written into memory.

Fig. 7 – $\overline{OE}$ (DELAYED WRITE) CYCLE

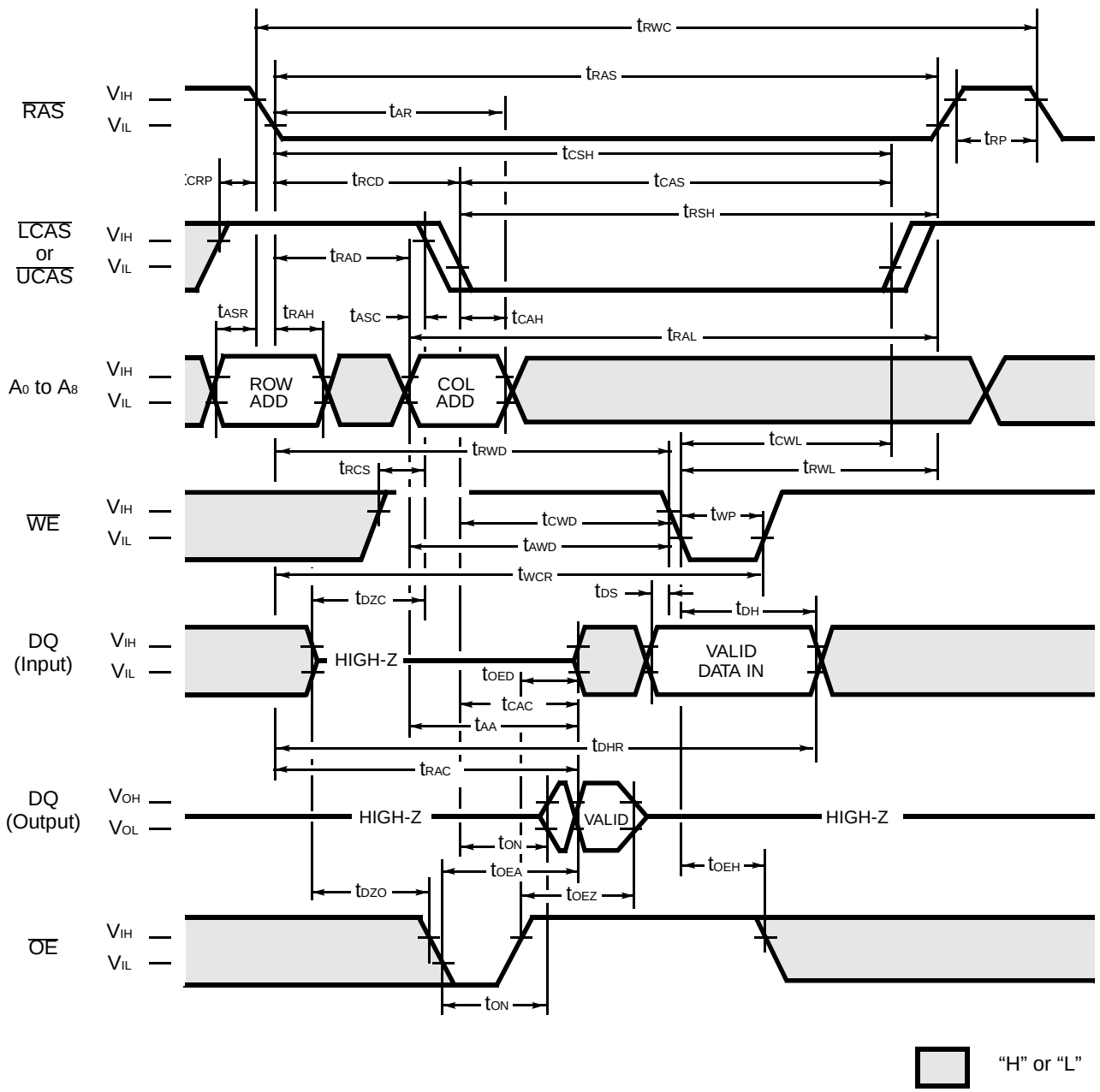


DESCRIPTION

In the $\overline{OE}$ (delayed write) cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

MB81V4260S-60/MB81V4260S-70

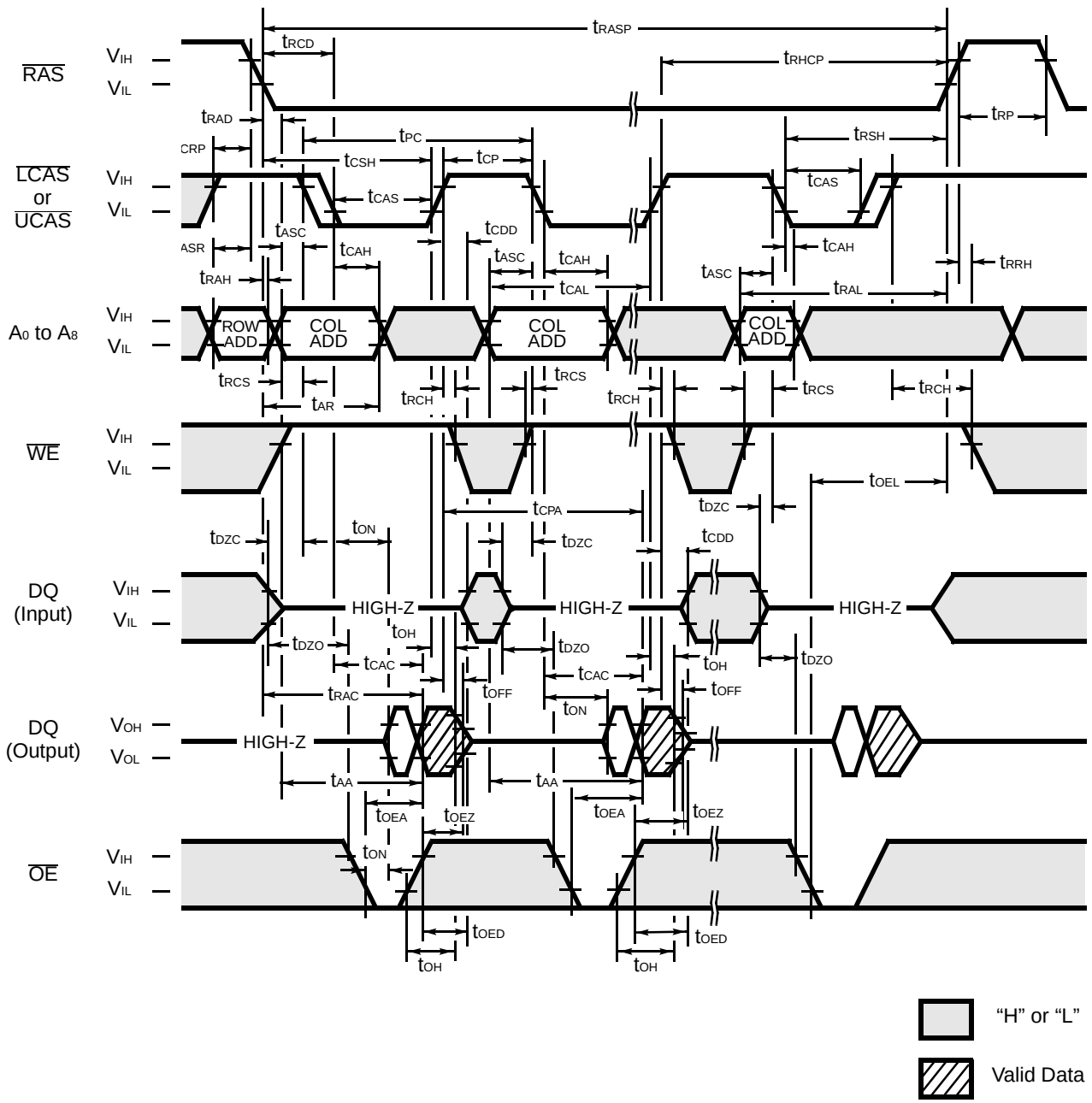
Fig. 8 – READ-MODIFY-WRITE-CYCLE



DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

Fig. 9 – FAST PAGE MODE READ CYCLE

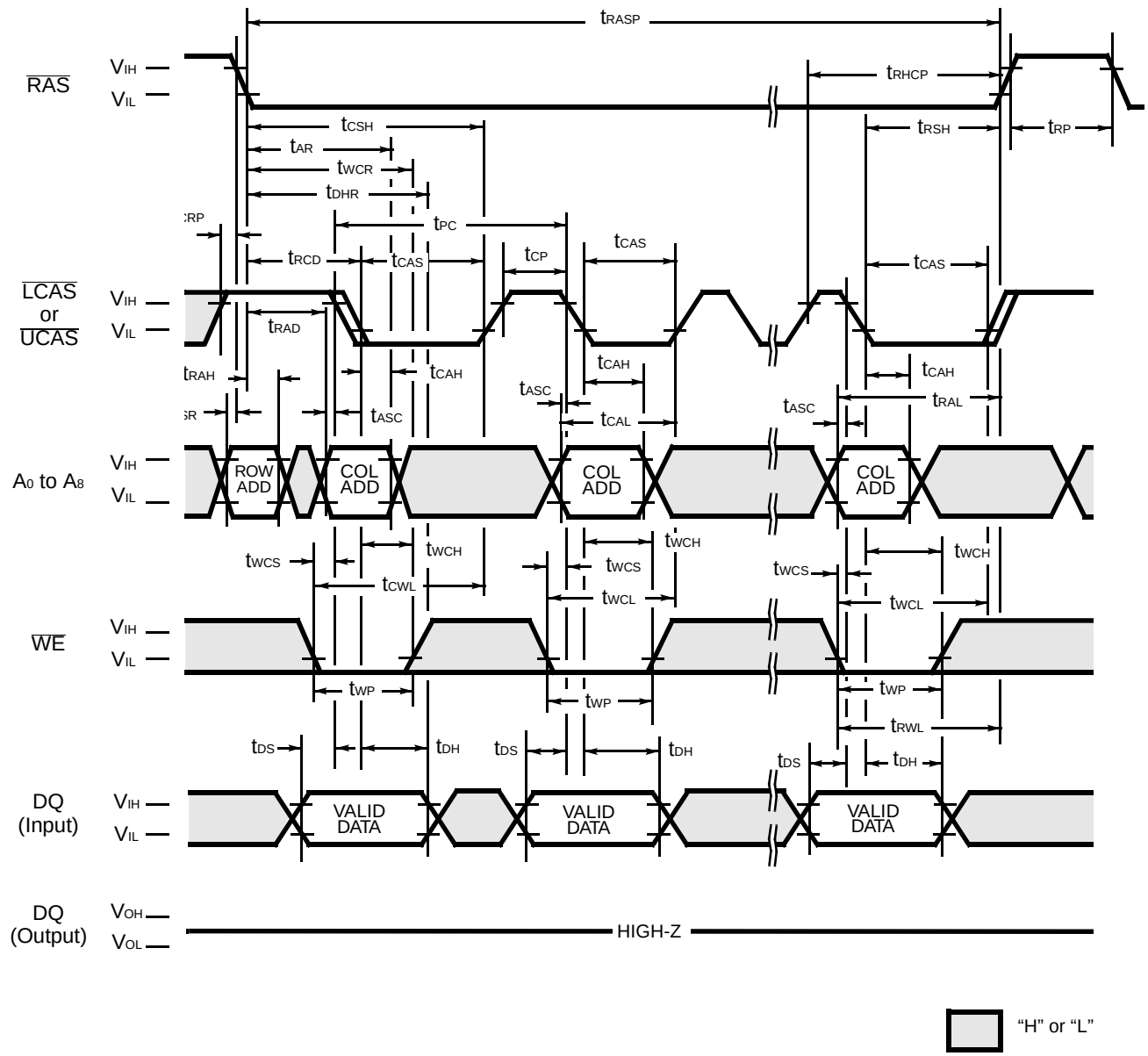


DESCRIPTION

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by t_{CAC}, t_{AA}, t_{CPA}, or t_{OEA}, whichever one is the latest in occurring.

MB81V4260S-60/MB81V4260S-70

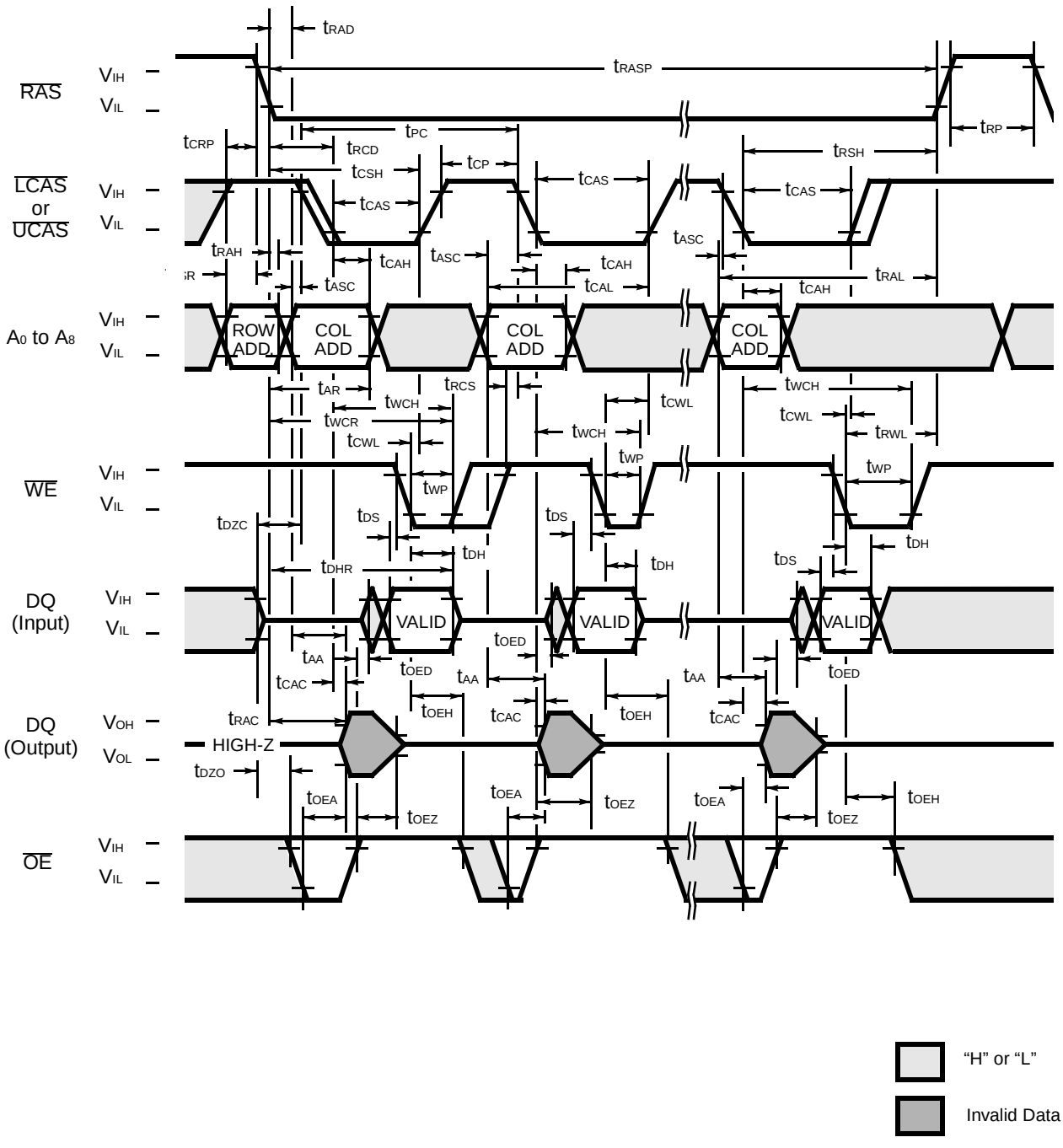
Fig. 10 – FAST PAGE MODE WRITE CYCLE ($\overline{OE}$ = "H" or "L")



DESCRIPTION

The fast page mode write cycle is executed in the same manner as the fast page mode read cycle except the states of $\overline{WE}$ and $\overline{OE}$ are reversed. Data appearing on the DQ_1 to DQ_8 is latched on the falling edge of $\overline{LCAS}$ and one appearing on the DQ_9 to DQ_{16} is latched on the falling edge of $\overline{UCAS}$ and the data is written into the memory. During the fast page mode write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, t_{CWL} must be satisfied.

Fig. 11 – FAST PAGE MODE $\overline{OE}$ WRITE CYCLE

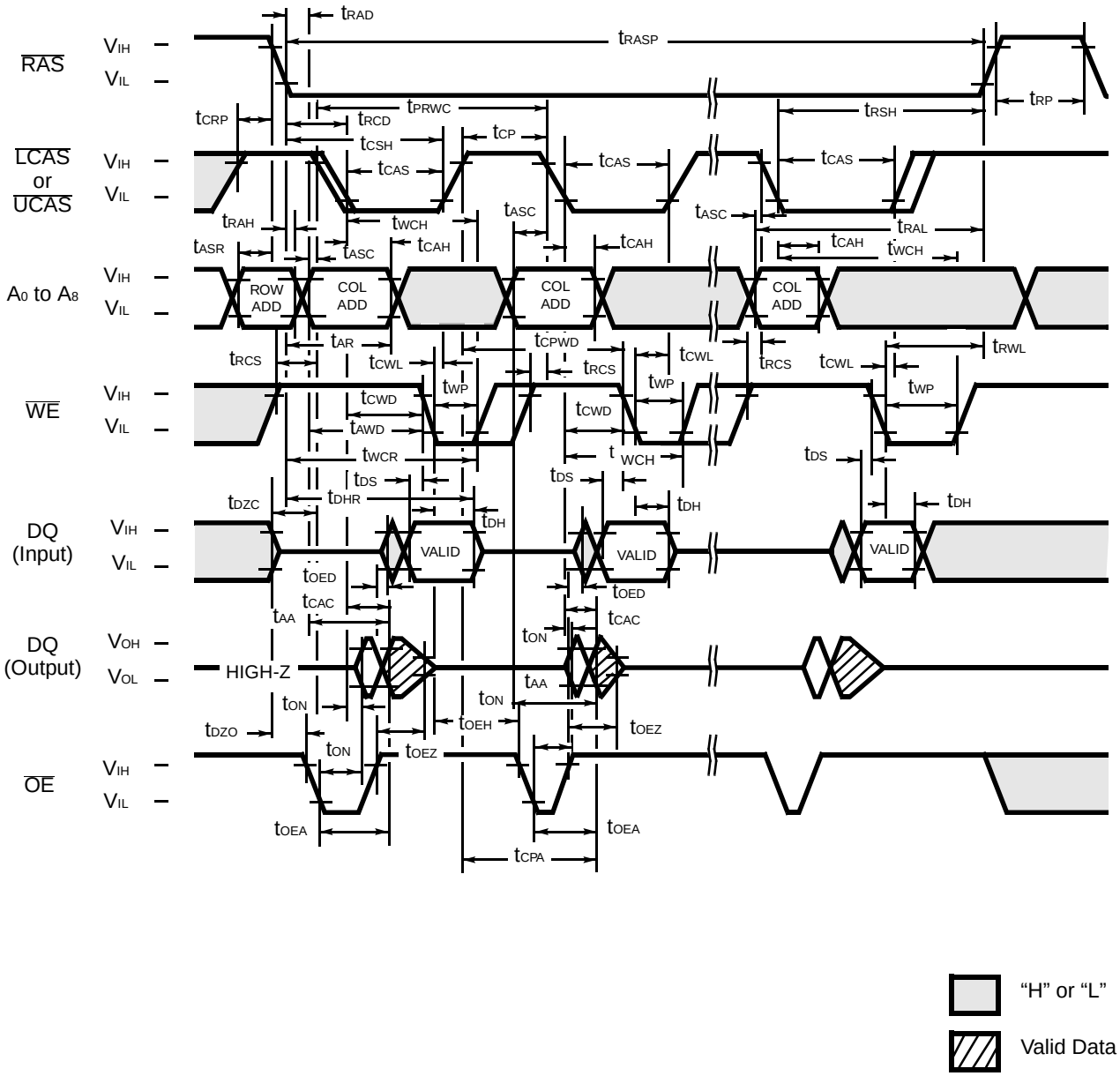


DESCRIPTION

The fast page mode $\overline{OE}$ (delayed) write cycle is executed in the same manner as the fast page mode write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the fast page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

MB81V4260S-60/MB81V4260S-70

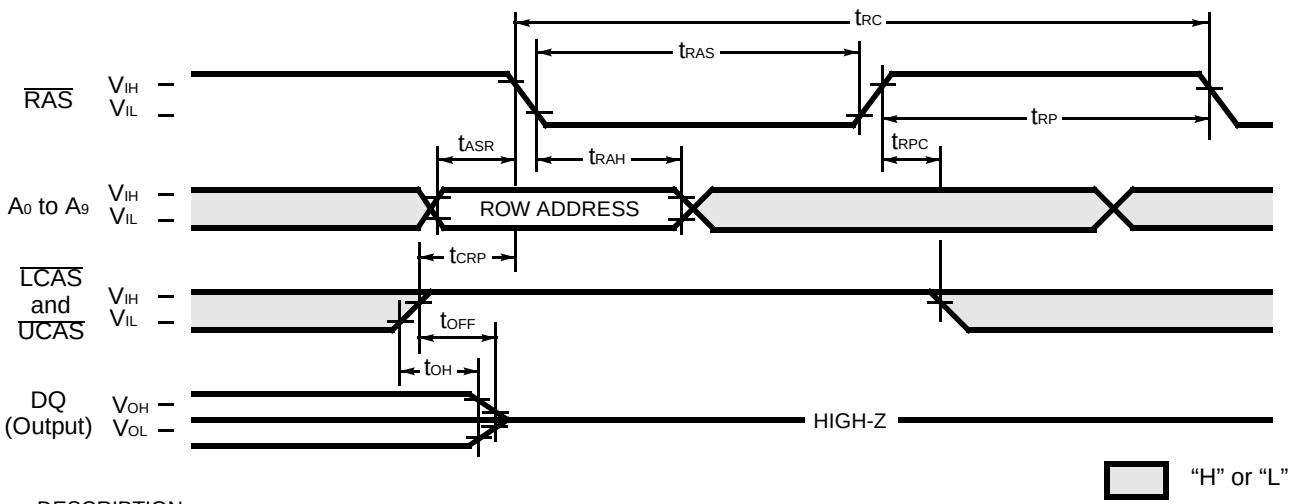
Fig. 12 – FAST PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During fast page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input date appears at the DQ pins during a normal cycle.

Fig. 13 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")

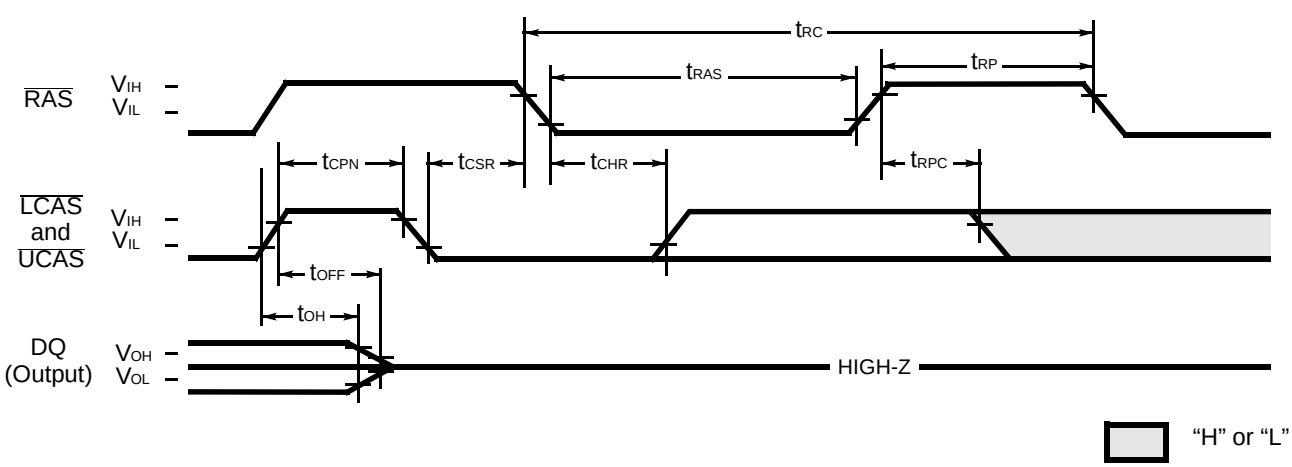


DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{LCAS}$ and $\overline{UCAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

Fig. 14 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")

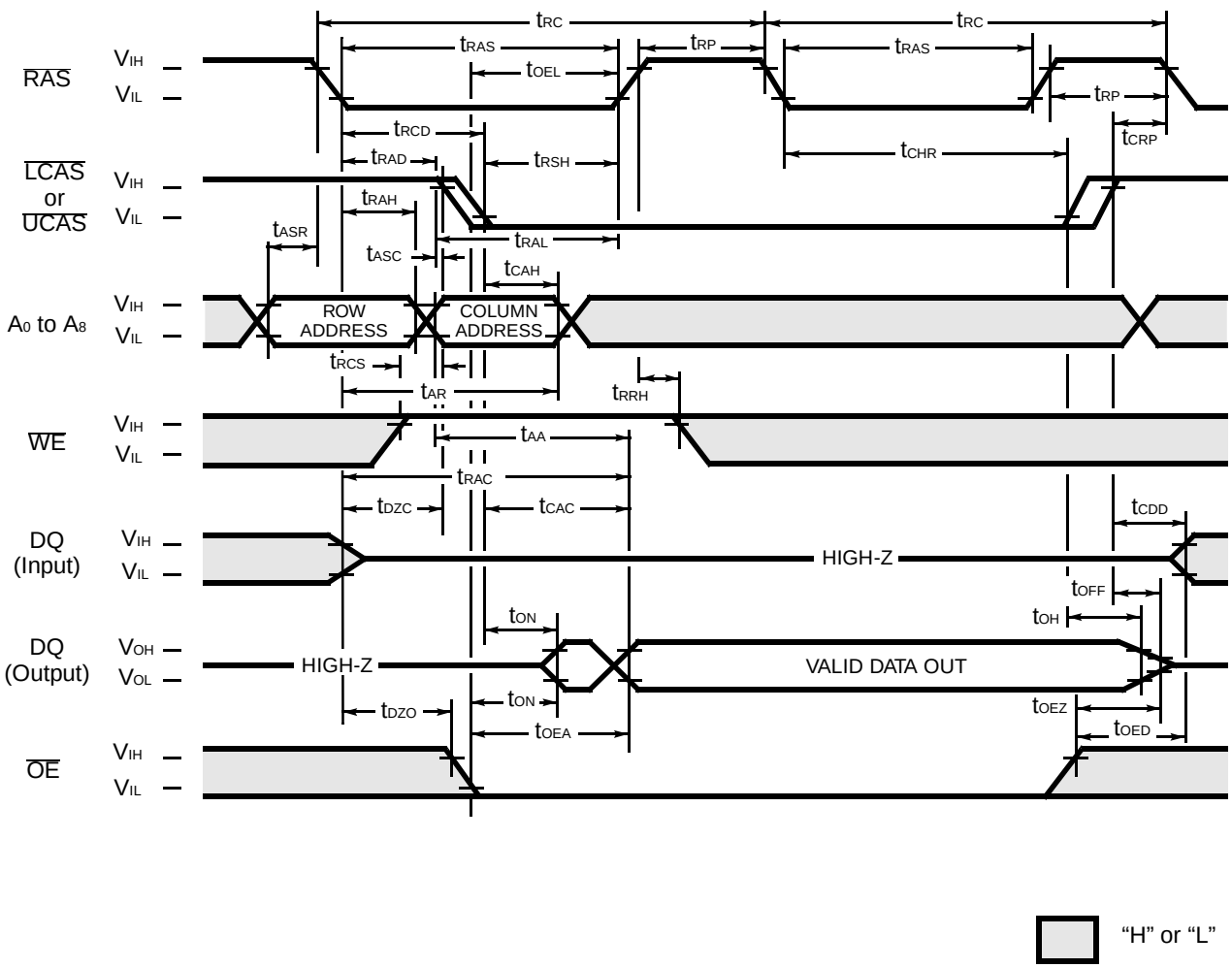


DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{LCAS}$ or $\overline{UCAS}$ is held Low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

MB81V4260S-60/MB81V4260S-70

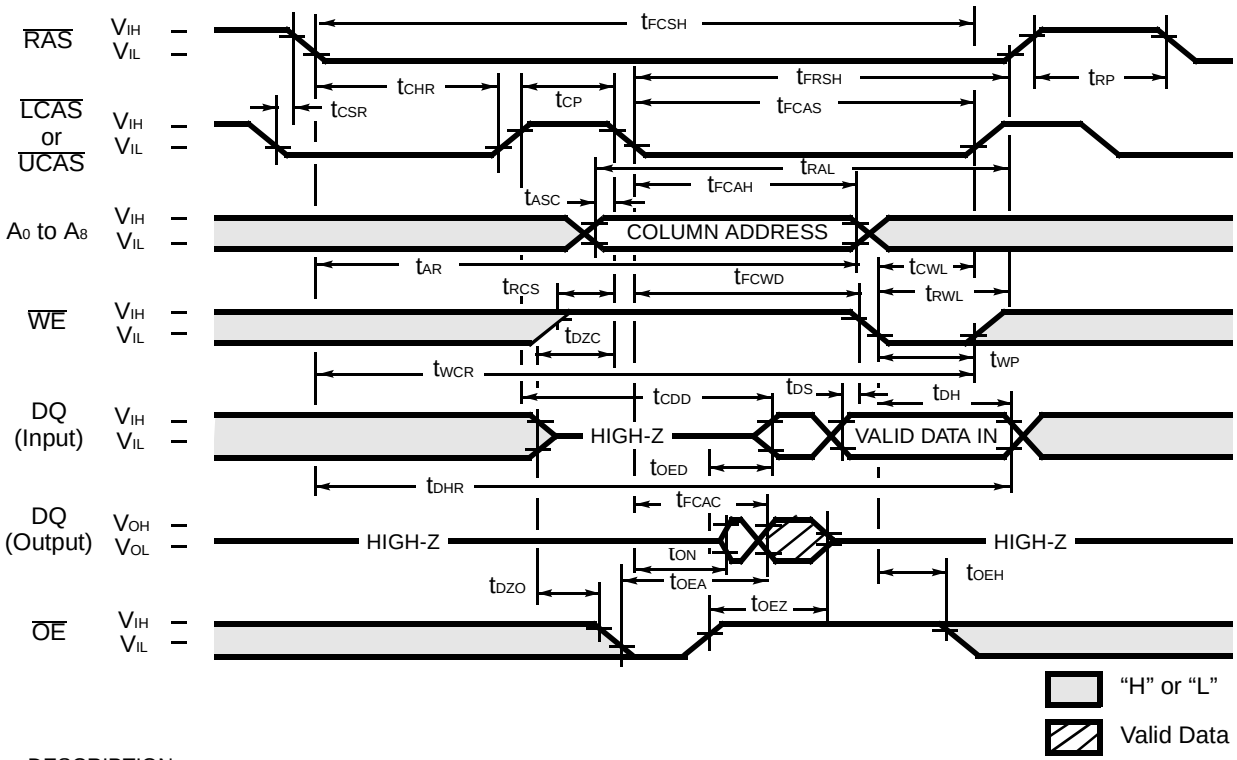
Fig. 15 – HIDDEN REFRESH CYCLE



DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling $\overline{\text{RAS}}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability.

Fig. 16 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. After a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, if $\overline{LCAS}$ or $\overline{UCAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits A_0 through A_8 are defined by the on-chip refresh counter.
Column Address: Bits A_0 through A_8 are defined by latching levels on A_0-A_8 at the second falling edge of $\overline{LCAS}$ or $\overline{UCAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

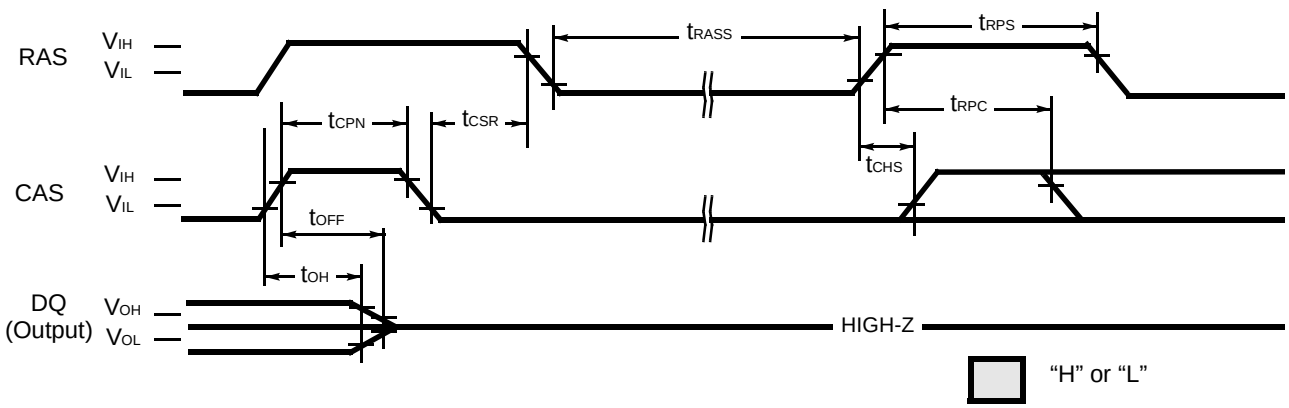
1) Normalize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 512 row addresses at the same column address by using CBR refresh counter test cycles.
4) Read "0" written in procedure 3) by using normal read cycle and check; After reading "0" and check are completed (or simultaneously), write "1" to the same addresses by using normal write cycle (or read-modify-write cycle).
5) Read and check data "1" written in procedure 4) by using CBR refresh counter test cycle for all 512 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
			Min.	Max.	Min.	Max.	
90	Access Time from $\overline{CAS}$	t_{FCAC}	—	55	—	55	ns
91	Column Address Hold Time	t_{FCAH}	30	—	30	—	ns
92	$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{FCWD}	80	—	80	—	ns
93	$\overline{CAS}$ Pulse width	t_{FCAS}	55	—	55	—	ns
94	$\overline{RAS}$ Hold Time	t_{FRSH}	55	—	55	—	ns
95	$\overline{CAS}$ Hold Time	t_{FCSH}	85	—	85	—	ns

Note: Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Fig. 17 – SELF REFRESH CYCLE (A_0 - A_9 = $\overline{WE}$ = $\overline{OE}$ = "H" or "L")



(At recommended operating conditions unless otherwise noted.)

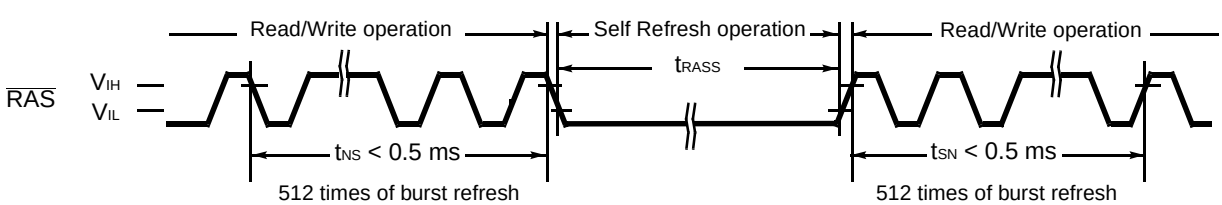
No.	Parameter	Symbol	MB81V4260S-60		MB81V4260S-70		Unit
			Min.	Max.	Min.	Max.	
100	$\overline{RAS}$ Pulse Width	t_{RASS}	100	—	100	—	µs
101	$\overline{RAS}$ Precharge Time	t_{RPS}	110	—	125	—	ns
102	$\overline{CAS}$ Hold Time	t_{CHS}	–50	—	–50	—	ns

Note: Assumes Self refresh cycles only.

DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter. If $\overline{CAS}$ goes to "L" before $\overline{RAS}$ goes to "L" (CBR) and the condition of $\overline{CAS}$ "L" and $\overline{RAS}$ "L" is kept for term of tRASS (more than 100µs), the device can be entered the self refresh cycle. And after that, refresh operation is automatically executed per fixed interval using internal refresh address counter during "$\overline{RAS}$=L" and "$\overline{CAS}$=L".
And exit from self refresh cycle is performed by toggling of $\overline{RAS}$ and $\overline{CAS}$ to "H" with specifying t_{CHS} min.
Restruction for Self refresh operation ;
For self refresh operation, the notice below must be considered.

1) In the case that distribut CBR refresh are operated in read/write cycles
   Self refresh cycles can be executed without special rule if 512 cycles of distribut CBR refresh are executed within t_{REF} max..
2) In the case that burst CBR refresh or $\overline{RAS}$ only refresh are operated in read/write cycles
   512 times of burst CBR refresh or 512 times of burst $\overline{RAS}$ only refresh must be executed before and after Self refresh cycles.

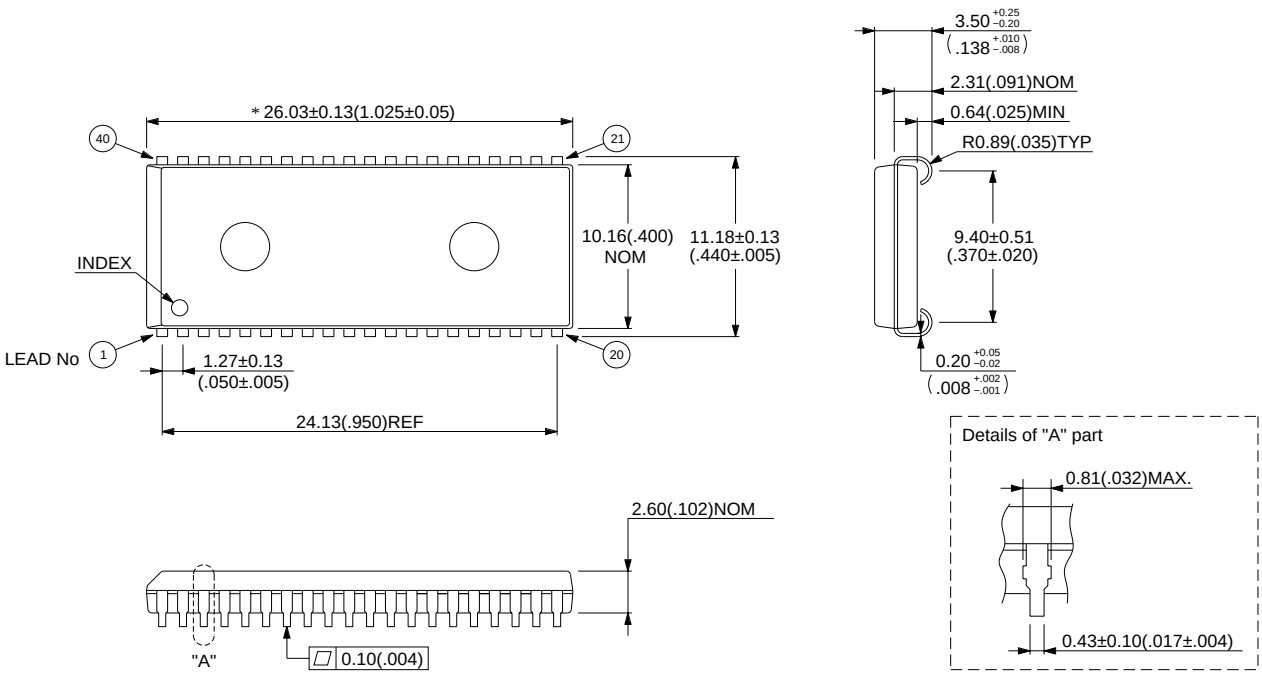


■ PACKAGE DIMENSIONS

(Suffix: -PJ)

40-pin plastic SOJ
(LCC-40P-M01)

*: Resin protrusion. (Each side:0.15(.006)max)



Dimensions in mm (inches)

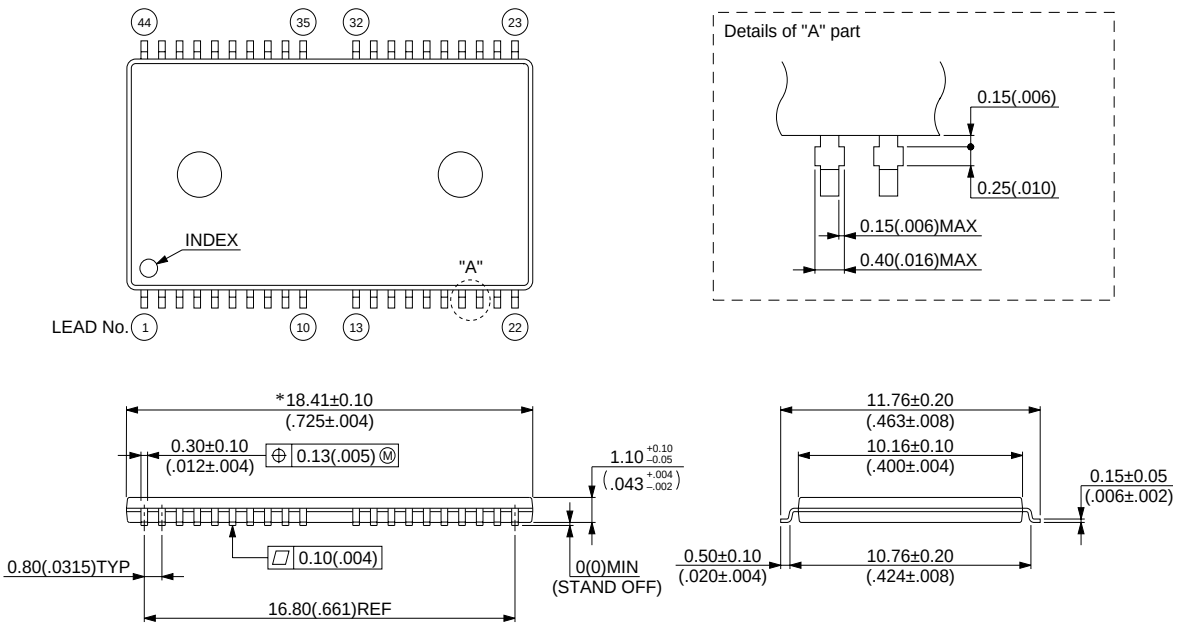
(Continued)

MB81V4260S-60/MB81V4260S-70

(Suffix: -PFTN)

44-pin plastic TSOP (II)
(FPT-44P-M07)

*: Resin protrusion. (Each side:0.15(.006)max)



Dimensions in mm (inches)

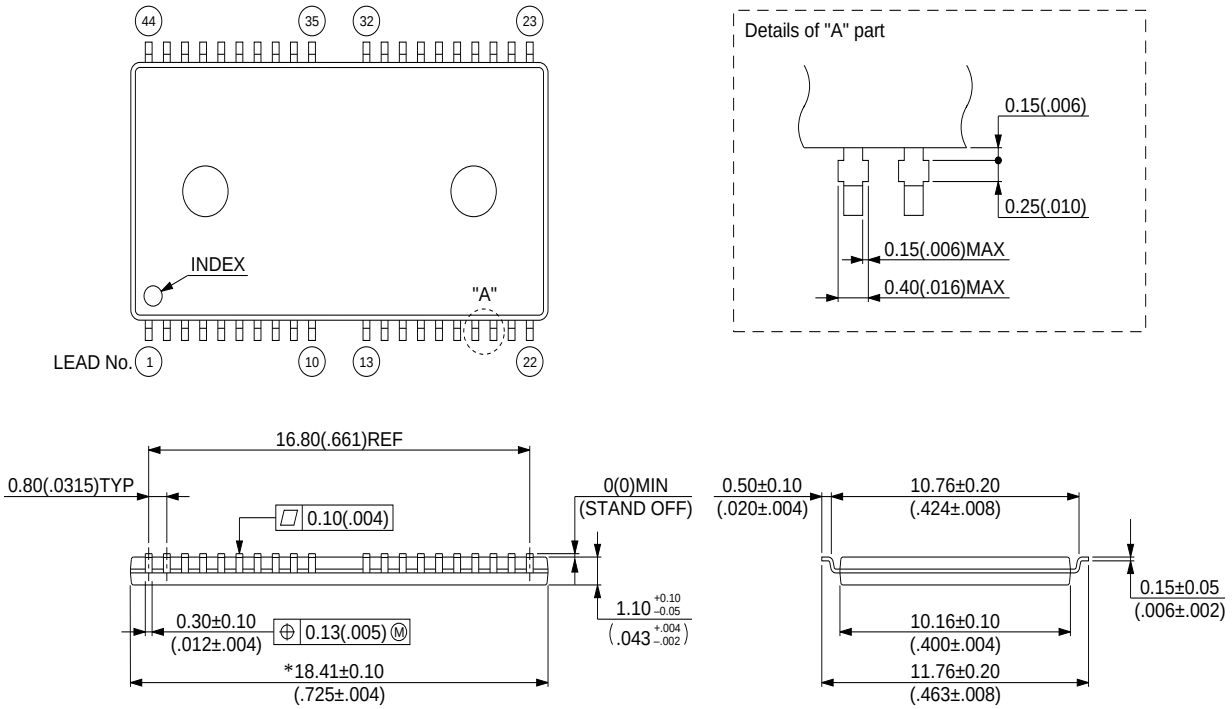
(Continued)

(Continued)

(Suffix: -PFTR)

44-pin plastic TSOP (II)
(FPT-44P-M08)

*: Resin protrusion. (Each side:0.15(.006)max)



Dimensions in mm (inches)

MB81V4260S-60/MB81V4260S-70

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